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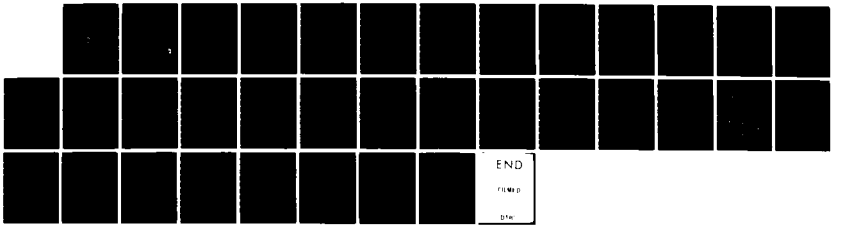

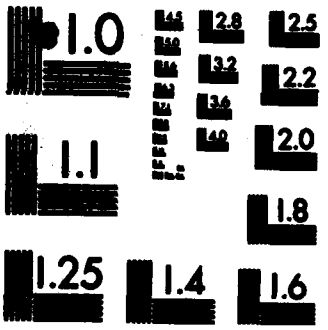

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ELECTRICAL PROPERTIES OF 10-50 nm TEOS LPCVD FILMS

AD-A146 416

TECHNICAL REPORT

R. H. VOGEL, S. R. BUTLER, AND F. J. FEIGL

24 AUGUST 1984

U. S. ARMY RESEARCH OFFICE

CONTRACT DAAG29-81-K-0007

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Electrical Properties of 10-50 nm TEOS LPCVD Films

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Abstract

Silicon dioxide films deposited at 700°C from the pyrolytic decomposition of tetraethoxysilane in a low pressure nitrogen ambient exhibited very poor electrical properties. This was due to the poor quality of both the LPCVD oxide bulk (manifest as a hysteretic instability exceeding one Volt in 20 nm films) and the LPCVD oxide-silicon interface (interface trap charge and fixed charge exceeding 10^{12} cm^{-2}). These were not improved by post-deposition annealing in nitrogen at 700°C. However, the interface characteristics were improved by post-deposition annealing in oxygen. Silicon dioxide deposited at 700°C from the pyrolytic decomposition of tetraethoxysilane in a low pressure oxygen ambient exhibited reduced values of interface trap charge and fixed charge, and an order of magnitude smaller bias instability. The interface properties of these films could be further improved by standard N_2-PDA/PMA annealing sequences known to be beneficial for thermal oxides.

Table of Contents

Electrical Properties of 18-50 nm TEOS LPCVD Films

1 Introduction

We have examined the electrical properties of MOS capacitor structures incorporating dielectrics formed by low pressure chemical vapor deposition (LPCVD) of silicon dioxide on single crystal silicon substrates. The specific LPCVD process studied was the pyrolysis of tetraethoxysilane (TEOS, also called tetraethylorthosilicate) at 700°C. A commonly reported method for TEOS LPCVD involves introducing liquid-source TEOS into a reactor via an inert carrier gas, commonly N_2 [1, 2]. We have investigated this method, and a modified method involving an O_2 carrier.

The objective of this research was to develop low-temperature processing sequences which improved the quality of deposited oxides in the 10-50 nm thickness range appropriate to very-large-scale-integration (VLSI) technology. Low fabrication temperature is a requirement which VLSI scaling imposes on insulator technology [3]. In the present study, all oxide processing was carried out at temperatures below that required for dry thermal oxidation of silicon (i. e., below 800 ^{o}C). TEOS was chosen for this investigation because it is readily available as an electronic grade liquid source material. TEOS dielectric films are widely used for device passivation or isolation, and the basic processing of these films is straightforward, economical, and well-documented [1, 2, 4, 5].

However, pyrolytic silicon dioxide films generally exhibit electrical properties which "do not meet the standard which is necessary for a good gate oxide" [6]. Some investigators have suggested that the pyrolytic oxide-silicon substrate interface is the specific problem, and that the quality of the pyrolytic oxide itself is good [6]. Others have indicated that TEOS forms poor quality oxides [4, 7]. This report on the TEOS process emphasizes results on the substrate-oxide interface. A second report concerns LPCVD oxide films produced from the reaction of dichlorosilane with nitrous oxide, and emphasizes results on bulk oxide trapping [8].

1.1 Personnel Involved in This Program

The TEOS LPCVD oxide films were produced in the Microelectronic Fabrication Facility of the Sherman Fairchild Laboratory at Lehigh University. The liquid source pyrolytic reactor described in Section 2 was designed and constructed specifically for this project by Professor Butler and Dr. Vogel, who together carried out the program of film deposition and device fabrication. The work was supported largely by funds from the present contract. The automated MOS capacitor measurement system described in Section 2 was also designed and constructed specifically for this project. The development of this system, and the entire program of capacitor characterization, was carried out by Dr. Vogel with the assistance of Dr. Titcomb.

Overall direction of this project was the responsibility of Professor Butler. Professor Feigl was responsible for the capacitor measurement program.

2 Experimental Details

An LPCVD reactor was constructed for the deposition of SiO_2

films from the pyrolytic decomposition of TEOS. This reactor is illustrated in Figure 1. The TEOS was introduced into the reactor via a saturated carrier gas passed through a bubbler containing a commercial liquid source. The carrier gas composition could be varied between 100% N_2 and 100% O_2 by varying the flow rates of the respective gasses. The TEOS source was maintained at constant temperature and pressure (the latter approximately one atmosphere) so that a precise control of the reactant partial pressure could be achieved. The pressure differential between the TEOS source (760 Torr) and the reactor (less than 2 Torr) was maintained across a needle valve (N1 in Fig. 1). The reactor pressure was controlled by the "downstream" introduction of N_2 via a second needle valve (N2 in Fig. 1). A flow of nitrogen or oxygen at one atmosphere pressure could be introduced into the reactor from the pump side (via solenoid valve S3). These gasses were used to purge the reactor during wafer loading (N_2) and to carry out in situ post deposition annealing treatments (N_2 and O_2).

The deposition parameters used in this study are listed in Table 1. LPCVD SiO_2 films were deposited on one ohm-cm, n-type, (100) polished silicon substrates. Selected substrates were thermally oxidized in situ at 700°C for 60 minutes prior to LPCVD SiO_2 deposition. Oxide film thicknesses were determined by capacitance measurements and ellipsometry. An array of circular gate electrodes of area $(1\text{-}2)\times10^{-3}cm^2$ was formed by vacuum

deposition of Al on the deposited SiO_2 surface.

Selected research specimens were given postdeposition and postmetallization annealing treatments. Postdeposition anneals (PDA) were performed in situ at 700°C in N_2 and/or O_2 ambients for 30 minutes. Postmetallization anneals (PMA) were carried out at 430°C in a forming gas ambient for 30 minutes.

C-V and I-V characteristics were determined using a Boonton 72A 1 MHz capacitance meter, a Keithley 602 electrometer, and a Keithley 26220 picoammeter. The capacitance meter was modified so that both 1 MHz high frequency C-V characteristics and quasi-static low frequency C-V characteristics could be measured simultaneously [9]. Bias-temperature-stress (BTS) measurements were carried out on a Temptronic TP-36 hot stage controlled by a PAR 410 C-V plotter. BTS studies were done at 150°C and 200°C with both positive and negative applied biases of approximately 1 $MV-cm^{-1}$.

The measuring instruments were interfaced to a microprocessor control system, as illustrated in Figure 2. A 16-bit digital-to-analog converter and a high voltage op-amp controlled by an INS8073 single board computer were used to generate a linear voltage ramp. Analog-to-digital conversion of the analog outputs from the capacitance meter, the electrometer/picoammeter, and the voltage ramp was accomplished via digital panel meters (DPM). The BCD outputs of the DPM's were

transmitted to a PDP 11/34 computer for analysis.

3 Experimental Results

Average oxide growth rates of 2.8 to 4.0 nm-min^{-1} were obtained with the deposition parameters listed in Table 1. The growth rate with an O_2 carrier gas was systematically less than the growth rate with an N_2 carrier gas, by approximately thirty percent. We used the TEOS LPCVD process to produce 10-75 nm thick films, uniform to within one percent on individual Si substrates. The growth rate decreased by fifty percent along the reactor axis and downstream from the gas inlet. This was due to depletion of the TEOS reactant partial pressure (see reference 2, pages 99 and 109).

Figure 3 exhibits three representative C-V curves for MOS capacitors incorporating TEOS LPCVD oxides deposited via a 100% N_2 carrier gas. In general, such unannealed oxides exhibited very poor and highly variable oxide-silicon interface quality. In addition to large interface trap densities (mid-gap D_{it} in excess of 10^{+12} cm^{-2}-eV^{-1}), these oxides exhibited complex room temperature bias instabilities, even at applied fields below 1 MV-cm^{-1}. Room temperature instabilities observed under high

applied fields are illustrated in Figure 4. Two distinct types of hysteretic instability, with opposite sense, were observed. The bias instability labeled TYPE 1 in Figure 4 consisted of a positive flat band shift when the device was ramped from accumulation to inversion, and a negative flat band shift when the device was ramped from inversion to accumulation. The TYPE 2 instability exhibited the opposite hysteretic sense (a negative flat band shift when the device was ramped from accumulation to inversion, for example). The instabilities observed in the N_2 deposited films varied considerably on both a sample-to-sample and a run-to-run basis, and were often a combination of the two types shown in Figure 4.

Selected substrates were subjected to an <u>in situ</u> thermal oxidation prior to LPCVD in a nitrogen carrier gas. This resulted in "dual-dielectric" structures consisting of 15-45 nm thick deposited silicon dioxide films on top of a (5±1)nm thick thermal silicon dioxide layer. Figure 5 exhibits representative C-V curves obtained on MOS capacitors incorporating these dual dielectric structures. It is apparent from Fig. 5, Curve A, that the N_2-carrier LPCVD oxide/thermal oxide structures exhibited lower D_{it} values than the N_2-deposited oxide single dielectric layer structures (see Fig. 3). This procedure for improving the dielectric oxide-silicon interface has been suggested by previous investigators [6]. However, these films exhibit highly exaggerated TYPE 2 bias instabilities at room temperature (Fig.

5, Curves B and C). This hysteresis is completely reversible and the voltage shift between curves B and C can occur within a one second time period.

The overall quality of MOS structures with LPCVD oxide dielectrics was improved by the addition of O_2 to the TEOS carrier gas. Mid-gap D_{it} values averaged approximately $5x10^{+12}cm^{-2}-eV^{-1}$ for 100% N_2 carrier, and were highly variable. For 100% O_2 carrier, mid-gap D_{it} values were reproducibly less than $5x10^{11}cm^{-2}-eV^{-1}$. The decrease in D_{it} with increasing O_2 concentration was evident in the quasi-static C-V data (see Figure 6).

As-fabricated V_{FB} values were measured on MOS capacitors which had received no annealing treatments. If represented as oxide fixed charge Q_f/q [10], these values averaged $6x10^{+11}cm^{-2}$, and varied between $4x10^{+11}cm^{-2}$ and $10x10^{+11}cm^{-2}$ for the unannealed deposited oxides. However, there was no systematic variation of Q_f/q with deposition rate or with carrier gas composition, and the variability observed could be due to the D_{it} fluctuations, since the effects of these two charge components are not separable when both are large [11, 12].

In addition to the improvement in the SiO_2-Si interface quality, increasing the O_2 concentration in the TEOS carrier gas resulted in a significant reduction in the room temperature bias instabilities described above. The application of 4 $MV-cm^{-1}$

across 20 nm oxides deposited from N_2 and O_2 carrier gasses produced flat band voltage shifts of 1.3 V and 0.14 V, respectively.

All results thus far described were obtained on unannealed oxides and on MOS capacitors which had received no post-metallization annealing treatments. A complete post-deposition and post-metallization annealing study was also carried out, on LPCVD oxides deposited in both 100% N_2 and 100% O_2 carrier gasses. The three oxidation conditions used were those described in Section 2: (A) 100% O_2 PDA at 700°C, (B) 100% N_2 PDA at 700°C, and (C) forming gas PMA at 430°C. The effects of all possible annealing combinations were studied (A, A+B, A+B+C, B, B+C, C).

For oxides deposited in an N_2 carrier, annealing sequences not including O_2 PDA produced no reduction in either D_{it} or Q_f/q. However, annealing sequences including O_2 PDA produced significant reduction of both D_{it} and Q_f/q, as indicated in Figure 7. Note that the resulting oxides were still of very poor quality. Also, no 700°C annealing treatment significantly influenced the room temperature bias instabilities obvserved in these films.

For oxides deposited in an O_2 carrier, annealing treatment A produced no significant effect on the MOS electrical properties. The other annealing treatments, however, did produce a

significant improvement in both Q_f/q and D_{it}. This is illustrated in Figure 8, which shows the effect of the two annealing sequences B and B+C. The net result of the B+C sequence was a one-third reduction of the midgap trap density D_{it}. Such effects were previously reported for standard thermal oxides produced at temperatures in the vicinity of 1000°C [11-13].

4 Discussion of Results

The results presented here are consistent with the previous suggestion that deposited oxide films produced at low temperature and low vapor pressure in nitrogen ambients form a poor quality interface with silicon [6]. Pronounced ledges sometimes appeared in the high-frequency C-V characteristics of such oxides (Fig. 3). These have been attributed to the emission of interface trapped charge [14, 15].

The hysteresis effects observed in these samples were also complex and inconsistent. The Type I hysteretic instability sometimes observed (Fig. 4) could have been the result of filling and emptying electron traps located spatially within a tunneling distance of the Si-SiO_2 interface and located energetically at or near the silicon surface band gap. This phenomenon appeared to

be field dependent. The more commonly observed Type II hysteretic instability occured at moderate bias fields (1-4 MV-cm_{-1}) at room temperature. The sense of Type II hysteresis (C-V shifts to negative voltage after positive bias, as in Fig. 4) is consistent with positive ion instabilities [16] or dielectric polarization effects [17]. In the example illustrated in Figure 4, positive and negative bias stressing produced approximately symmetrical voltage shifts with respect to the as-grown device characteristic. This was expected for polarization effects [17], but it did not occur consistently in the present study and could have occured accidentally if mobile ions were involved (depending on the initial state of the oxide).

We do not understand the mechanism responsible for the Type II instability. However, this instability appeared to be associated with the poor bulk quality of these films, manifested in such properties as density, refractive index, and etch rate [1, 6, 18]. This hypothesis is supported by the fact that the films deposited in an oxygen carrier ambient, which have been shown to have bulk properties more closely approaching thermal oxides [19], do not exhibit the large bias instabilities observed in the films deposited in N_2 ambients.

An attempt at quantitative hydrogen impurity profiling of the LPCVD oxide films was not successful. The bulk concentration

of H-species in these films was too high to be quantified using the particular secondary ion mass spectrometric system employed (that of Dr. Charles Magee of the RCA Laboratories in Princeton, N. J.). This indicated an H-concentration exceeding $10^{21}cm^{-3}$, *i. e.*, approaching ten percent of the SiO_2 molecular concentration in bulk glassy silicon dioxide. This observation of high hydrogen species concentration in TEOS LPCVD oxides contradicted previous studies of infrared-active species such as OH and SiH [20]. The present results certainly indicated that hydrogen impurities could have accounted for bulk anomalies such as the Type II hysteretic instability.

When the deposited oxide was formed over a previously-grown thin thermal oxide, the large bias instability specifically associated with interface traps disappeared. Thus, the large voltage stretchout of the 1 MHz C-V curves displayed in Figure 3 are not present in the dual dielectric MOS devices. However, such devices exhibited a very large rigid room-temperature bias instability identical to the Type II hysteresis discussed in the previous paragraphs. The sign of this effect -- C-V shifts to positive voltage after negative bias, as in Fig. 5 -- was opposite to that previously described as a dual-dielectric instability. The conventional dual-dielectric instability has been attributed to injected charge carrier trapping at the deposited insulator-thermal oxide interface [4, 21]. Further, it was not possible to explain the effect observed in the present

study as a polarization phenomenon similar to that in single phosphosilicate glass dielectrics [7, 17]. The present effect was not symmetrical with positive and negative gate biases of equal magnitude, and occured within seconds at room temperature.

Thus, we do not understand the mechanism responsible for the Type II instability in LPCVD oxide-thermal oxide dual dielectric films. However, this instability again appeared be associated with the poor bulk quality of the LPCVD films. This conclusion is based on two observations: First, the Type II instability survived the above-noted improvement in the oxide-silicon interface produced by the addition of the thermal oxide layer. Second, the Type II instability was not observed in control capacitors fabricated on single layer thermal oxide films.

Previous investigators have shown that the overall physical and electrical properties of deposited silicon dioxide films can be improved by PDA treatment at approximately 1000°C [1, 6, 18]. PDA temperatures greater than the deposition temperature of 700°C were contrary to the objectives of the present work, however, and were not investigated. A common annealing sequence which has been shown to reduce Q_f and D_{it} in thermal oxides is a post-oxidation anneal in nitrogen at the growth temperature followed by PMA in forming gas. Similar sequences were applied to the LPCVD oxides.

PDA at 700°C in N_2, with or without PMA, had no significant

effect on the interface characteristics of LPCVD oxides deposited in N_2 carrier ambients. However, subjecting these oxides to PDA in an O_2 ambient produced a two-fold effect. First, O_2-PDA directly reduced both Q_f and D_{it} (Fig. 7, Curves A and B). Second, a subsequent N_2-PDA/PMA sequence further reduced these quantities (Fig. 7, Curves C and D).

5 Summary and Conclusions

Silicon dioxide films deposited at 700°C from the pyrolytic decomposition of tetraethoxysilane in a low pressure nitrogen ambient exhibited very poor electrical properties. This was due to the poor quality of both the LPCVD oxide bulk (manifest as a hysteretic instability exceeding one Volt in 20 nm films) and the interface between the LPCVD oxide and the silicon substrate (Q_f and mid-gap D_{it} of order $10^{12}cm^{-2}$).

The oxide-silicon interface was significantly improved by any one of three procedures which reduced both Q_f and D_{it}. These procedures were:

1. *In situ* exposure of the heated silicon substrate to an O_2 ambient before LPCVD (Fig. 5). This produced a thin thermal oxide interposed between the LPCVD oxide and the

substrate.

2. The addition of O_2 to the reactor ambient during LPCVD (Fig. 6). This probably involved surface adsorption of oxygen, which has been claimed to slow down other deposition reactions [22].

3. Exposure of the deposited oxide to an O_2 ambient after LPCVD (Fig. 7). This "anneal" treatment probably involved oxidation of the imperfectly formed interface between oxide and substrate.

In addition to direct improvement of interface quality, the use of 100% O_2 ambients during pyrolysis or PDA treatment made possible further reduction in both D_{it} and Q_f by standard N_2-PDA/PMA sequences (Fig. 8). Clearly, TEOS LPCVD oxide films exposed to O_2 at the deposition temperature have an SiO_2-Si interface more closely approaching that of a high temperature thermal oxide than TEOS LPCVD films exposed only to N_2.

The poor bulk quality of LPCVD oxide films produced by TEOS pyrolysis in an N_2 ambient was responsible for the Type II hysteretic instability (Fig. 4). This was not significantly affected by any of the annealing sequences studied by us. It was reduced an order of magnitude by pyrolysis in an O_2 ambient. Neither the origin of this instability, nor its reduction, is understood.

In summary, none of the oxide films produced by low-temperature LPCVD from a TEOS source approached the quality of high temperature thermal oxides. However, a troublesome feature of such oxide dielectric films, namely the poor quality of the oxide -silicon substrate interface, can be significantly improved if the deposition is carried out or terminated in an oxygen ambient.

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Table 1: Deposition Parameters in TEOS LPCVD

Reactor Temperature	700°C
Reactor Pressure	1.4 Torr
TEOS Partial Pressure	0.37 Torr
Carrier Gas Flow Rate	50 cc/min
Carrier Gas Composition	100% N_2 to 100% O_2
Deposition Times	7 to 30 min

List of Figure Captions

Figure 1. LPCVD deposition system: liquid TEOS bubbler; controls for nitrogen and oxygen carrier, annealing, and flushing gasses; low pressure deposition reactor and vacuum system. The following components of the gas handling system are illustrated: flowmeters (F), pressure gauges (G), manual control valves (V), solenoid control valves (S), needle valves (N), and regulator (R).

Figure 2. Schematic diagram of the automated C-V and I-V measurement system.

Figure 3. 1 MHz C-V curves obtained on MOS capacitors incorporating unannealed oxides deposited via a 100% nitrogen carrier gas. Three different oxide thicknesses are shown.

Figure 4. 1 MHz C-V curves obtained on MOS capacitors incorporating unannealed oxides deposited via a 100% nitrogen carrier gas. These oxides are relatively thick (40-45 nm). The two curves on a given plot illustrate room temperature bias instabilities observed after the application of ±4 MV/cm fields across the oxide. The hysteretic sense of Type I and Type II instabilities are indicated on the appropriate plot.

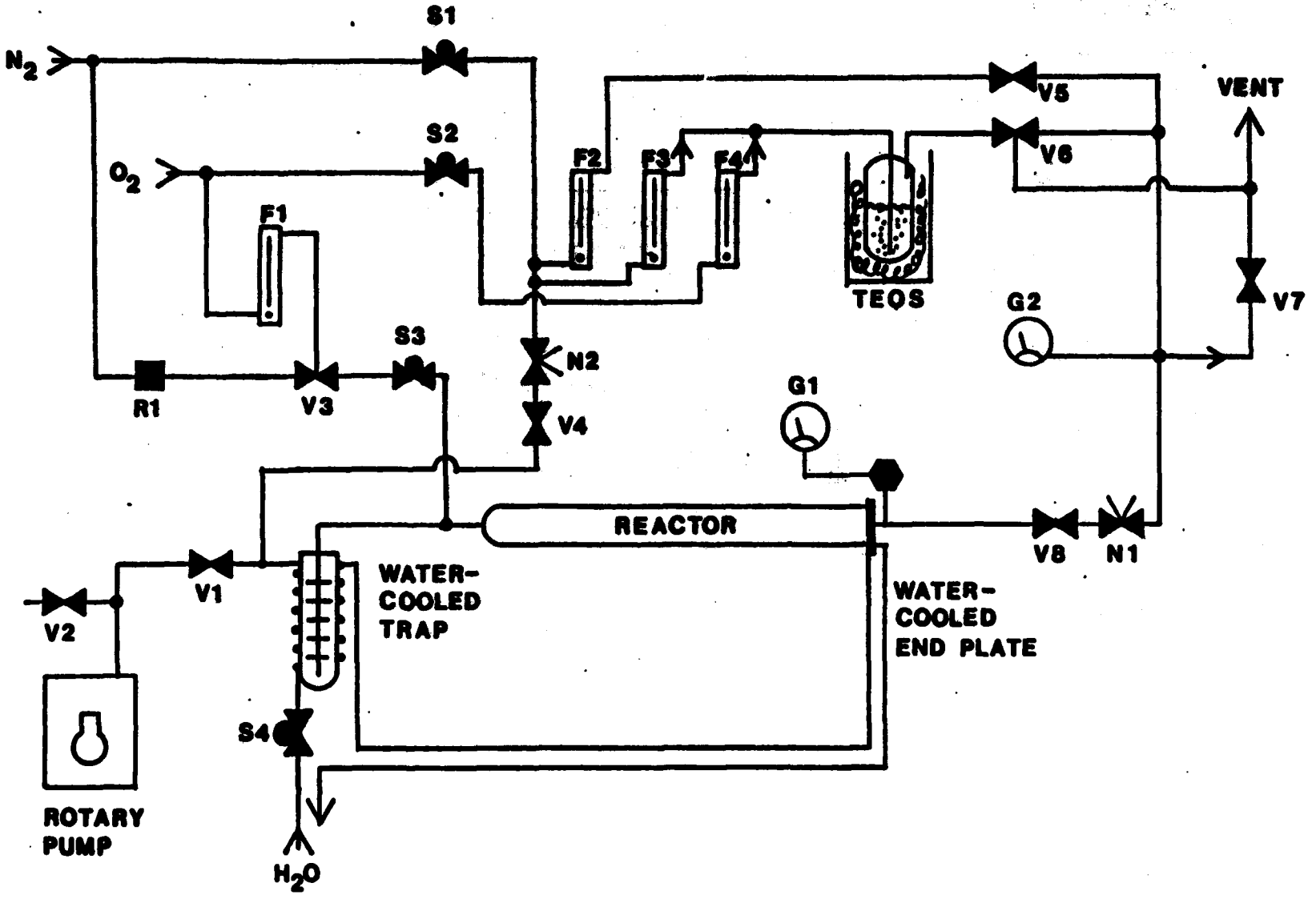
Figure 5. 1 MHz C-V curves obtained on an MOS capacitor incorporating a 28.5 nm thick two-layer silicon dioxide dielectric. The dielectric consisted of an LPCVD oxide deposited onto a 5 nm thick thermal oxide. The three C-V curves illustrate room temperature bias instability upon application of ±4 MV/cm fields across the oxide: (A) before application of bias, (B) after negative gate bias, and (C) after positive gate bias. This is a Type II instability.

Figure 6. Quasi-static C-V curves obtained on MOS capacitors incorporating unannealed oxides deposited via mixed oxygen and nitrogen carrier gasses. Results for four different oxygen concentrations are shown. The quasi-static curves are labelled by the percentage of oxygen in the carrier gas mixture. Under nominally identical deposition conditions, oxide thicknesses decreased systematically with oxygen concentration: 38.5 nm for 0% oxygen, 37.5 nm for 10%, 28.0 nm for 50%, 16.5 nm for 100%.

Figure 7. The effect of annealing treatments on the 1 MHz C-V curves

obtained on MOS capacitors incorporating a 35 nm thick oxide deposited via a 100% nitrogen carrier gas: (A) no anneal, (B) oxygen PDA, (C) oxygen PDA plus nitrogen PDA, and (D) oxygen PDA plus nitrogen PDA plus PMA.

Figure 8. The effect of annealing treatments on the 1 MHz C-V curves obtained on MOS capacitors incorporating a 50 nm thick oxide deposited via a 100% oxygen carrier gas: (A) no anneal, (B) nitrogen PDA, and (C) nitrogen PDA plus PMA. The final values of mid-gap D_{it} and Q_f/q are indicated.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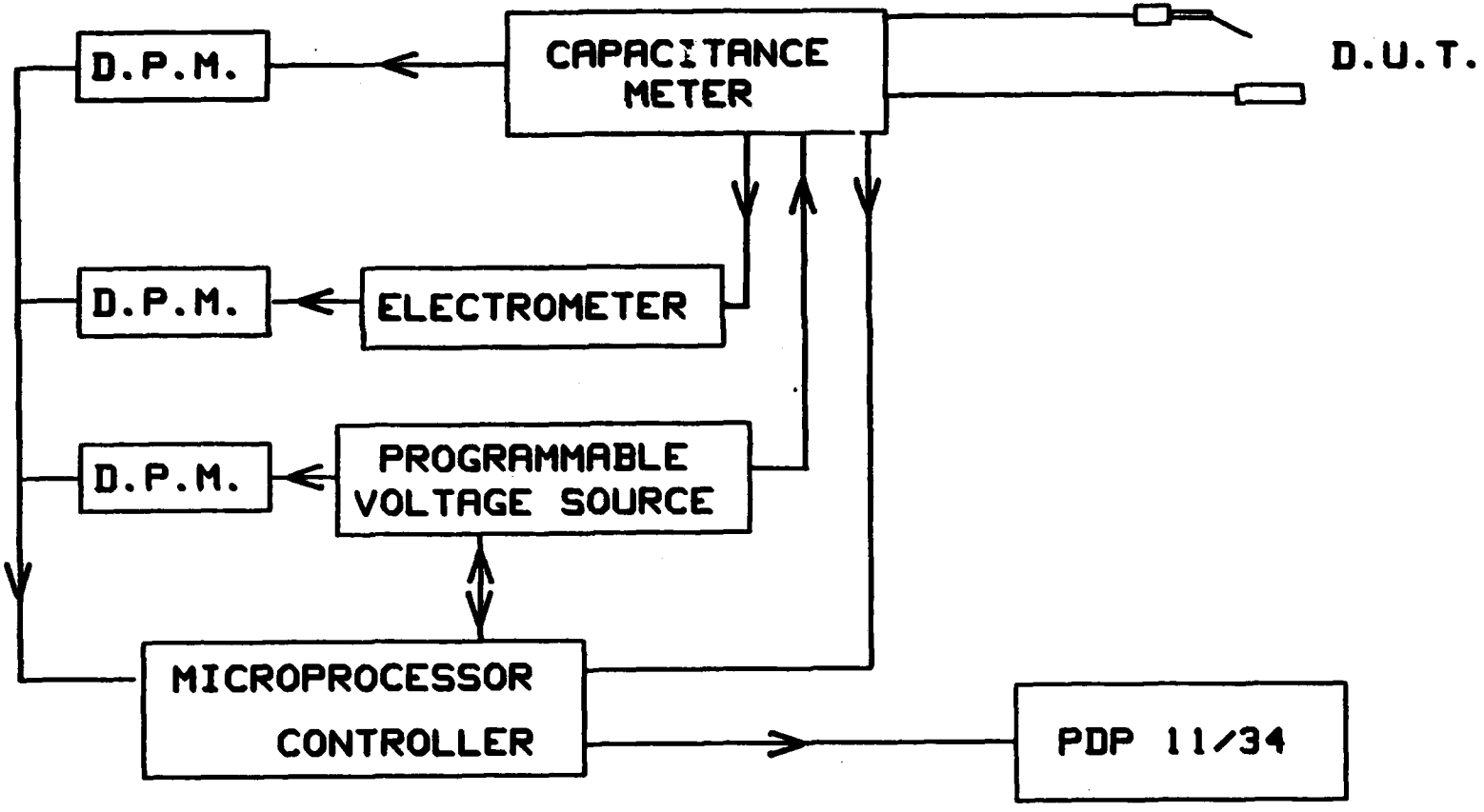
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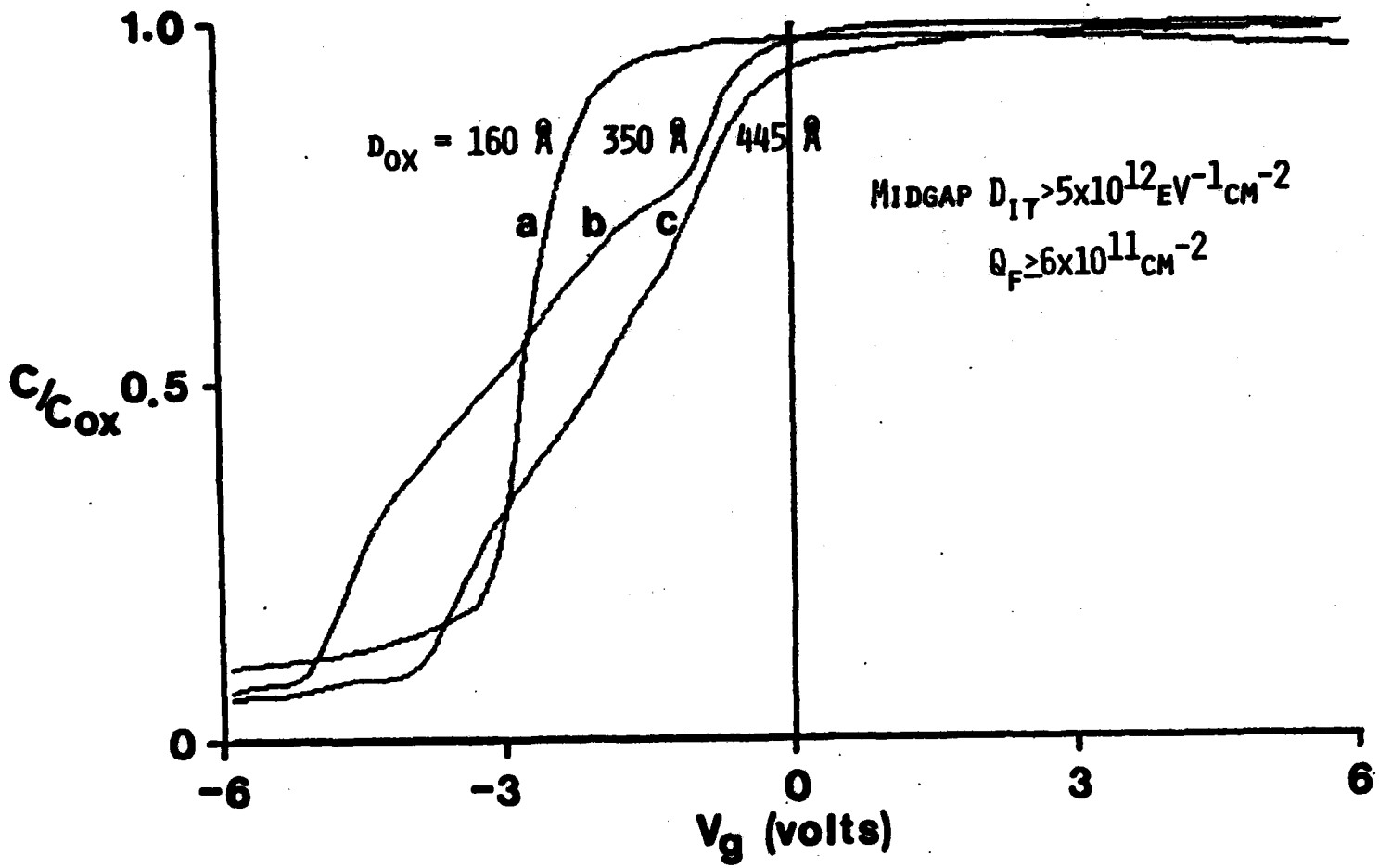
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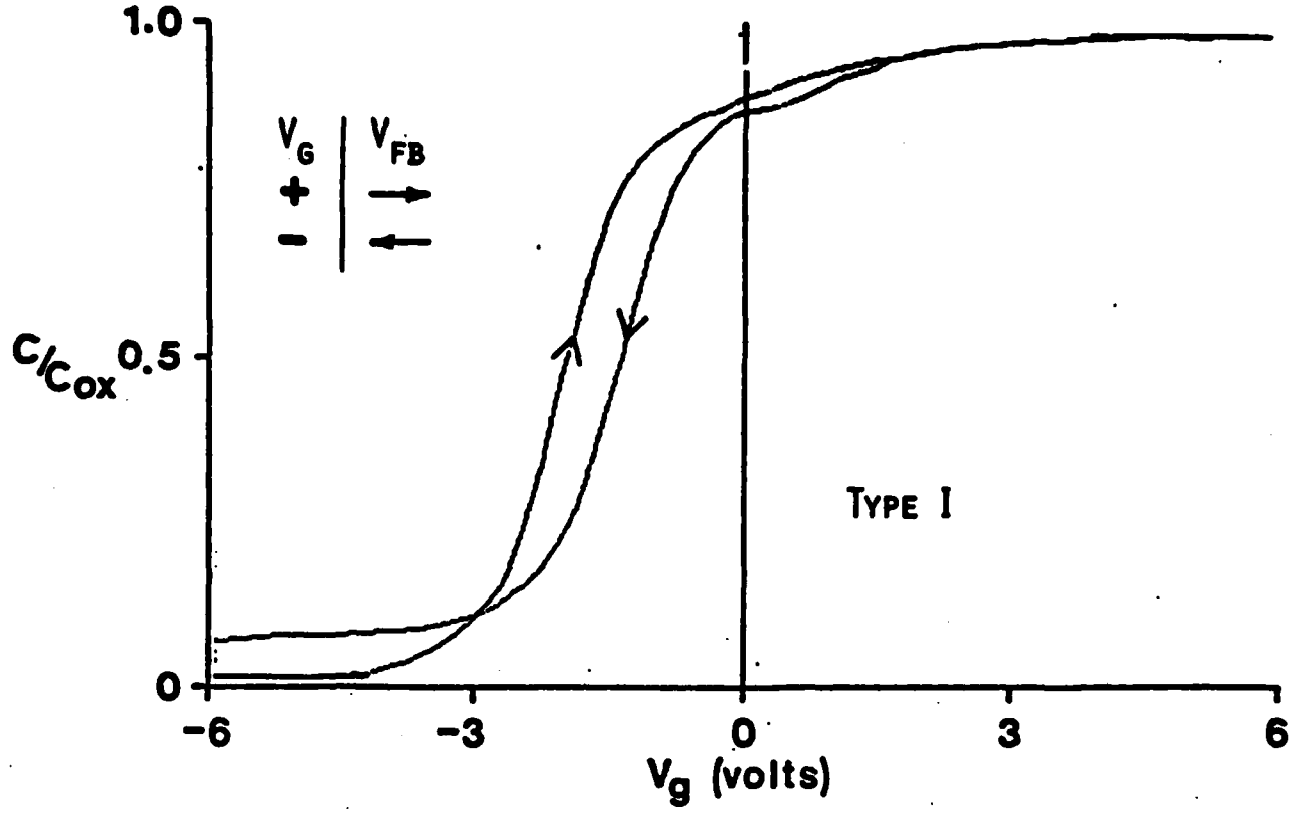
Fig. 3, p. 24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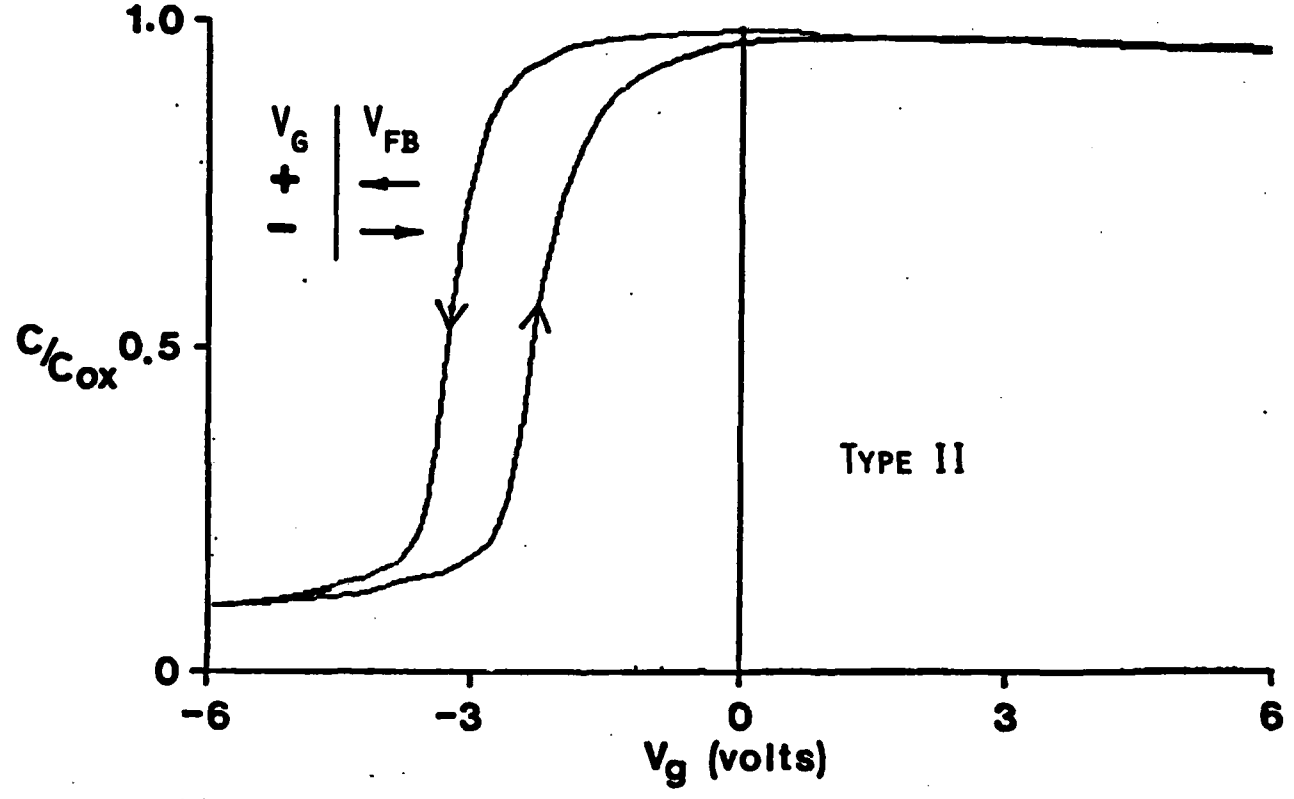
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Fig. 4, p. 25

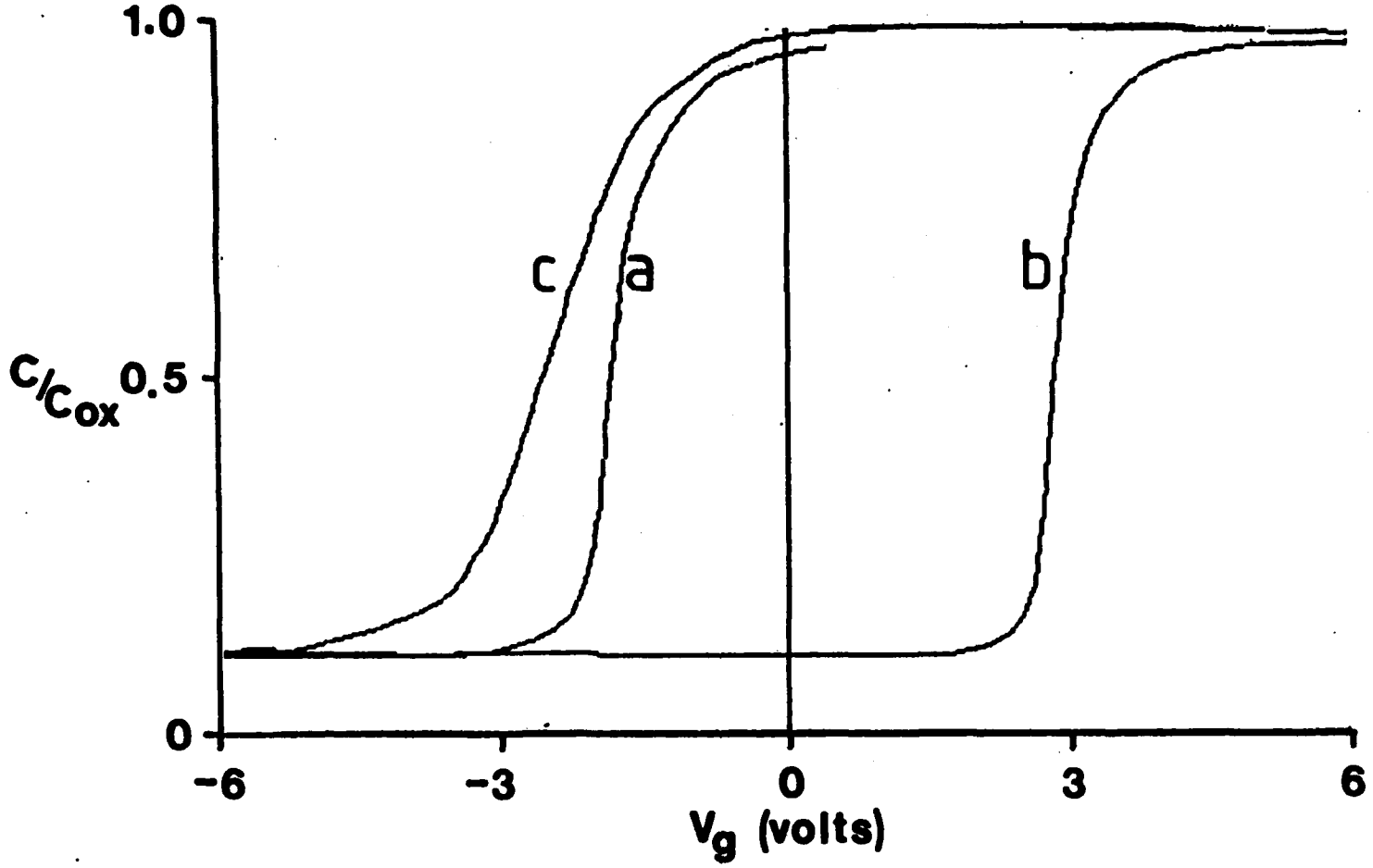

Fig. 5, p. 26

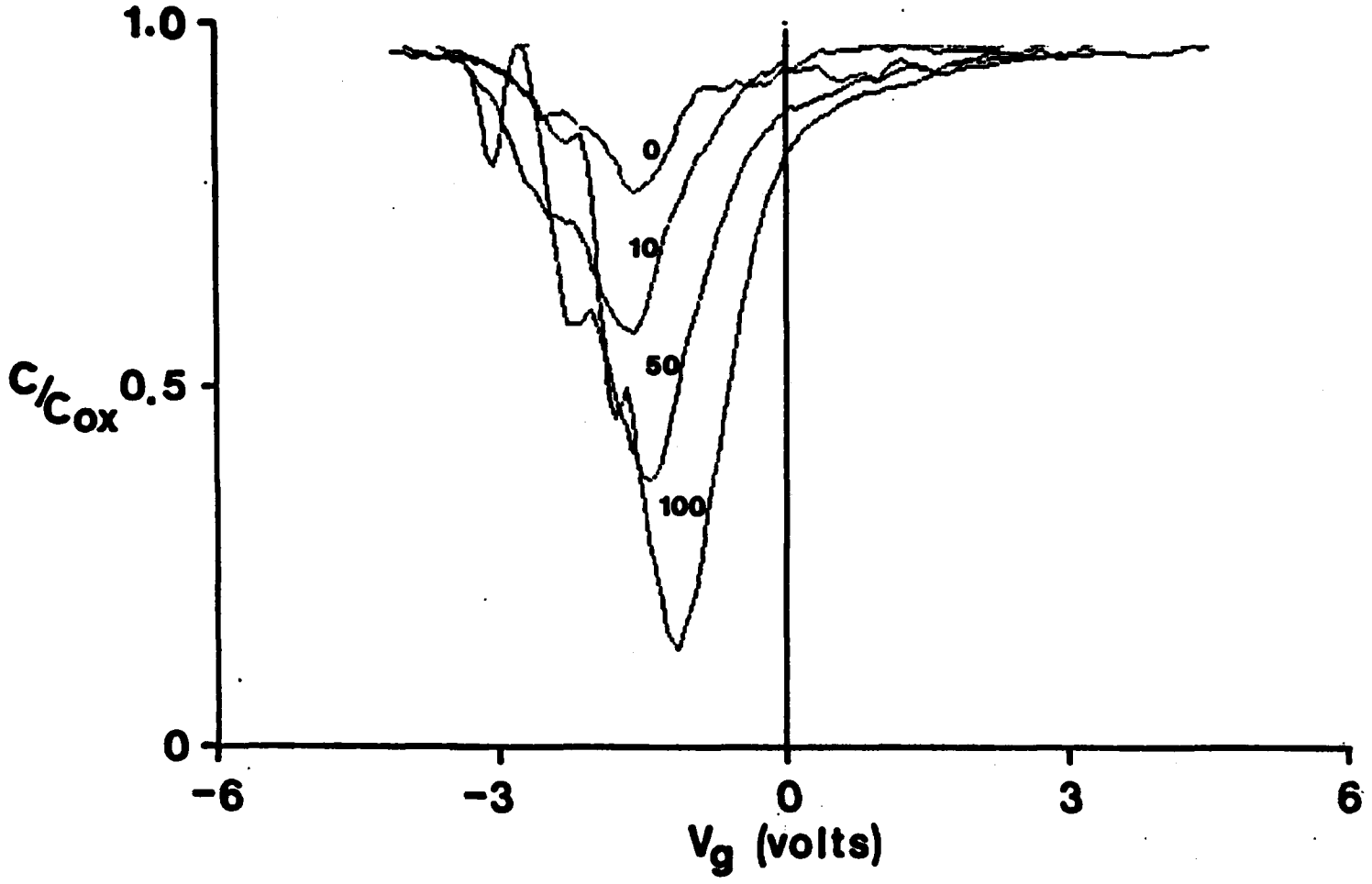

Fig. 6, p. 27

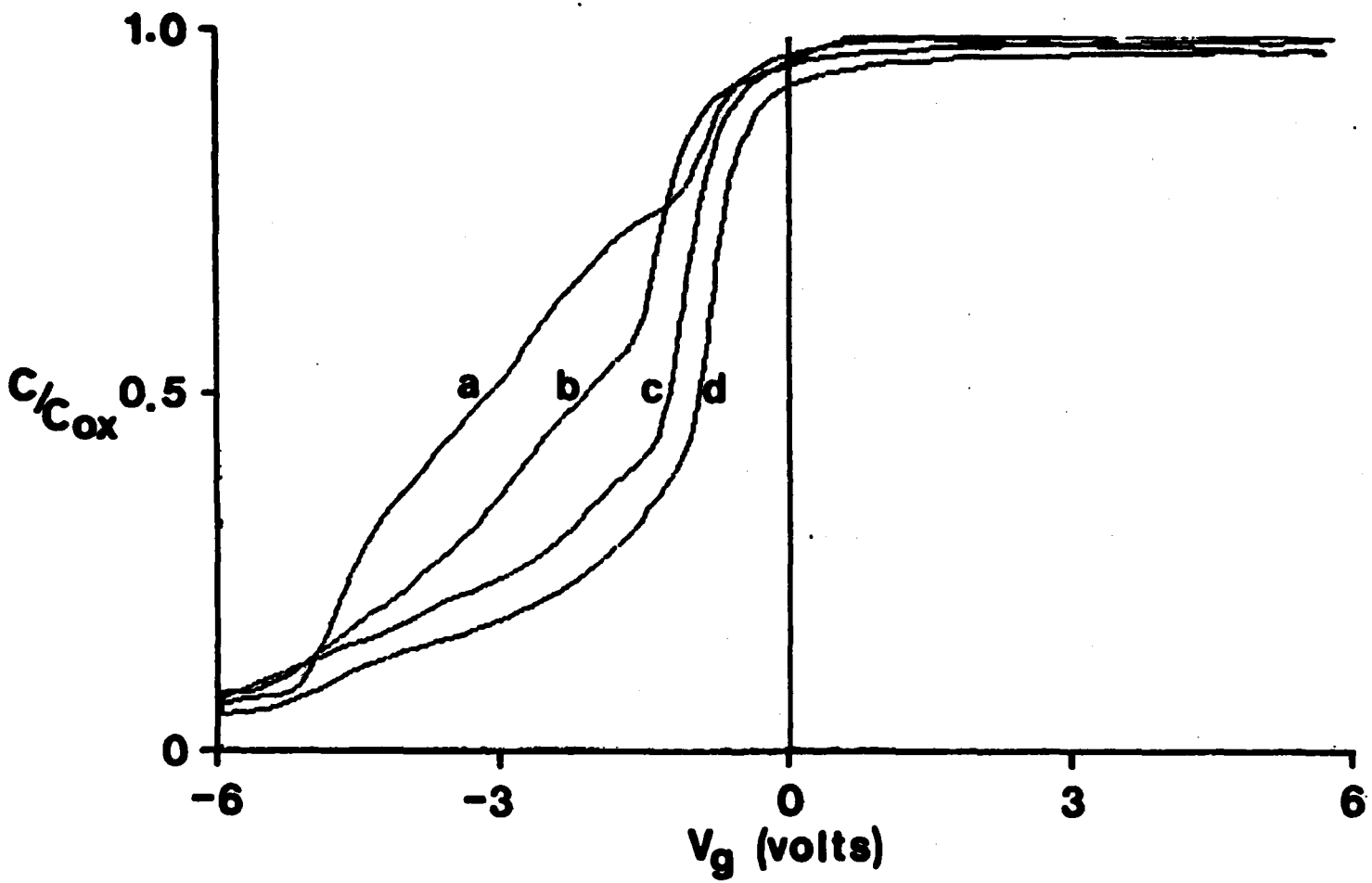

Fig. 7, p. 28

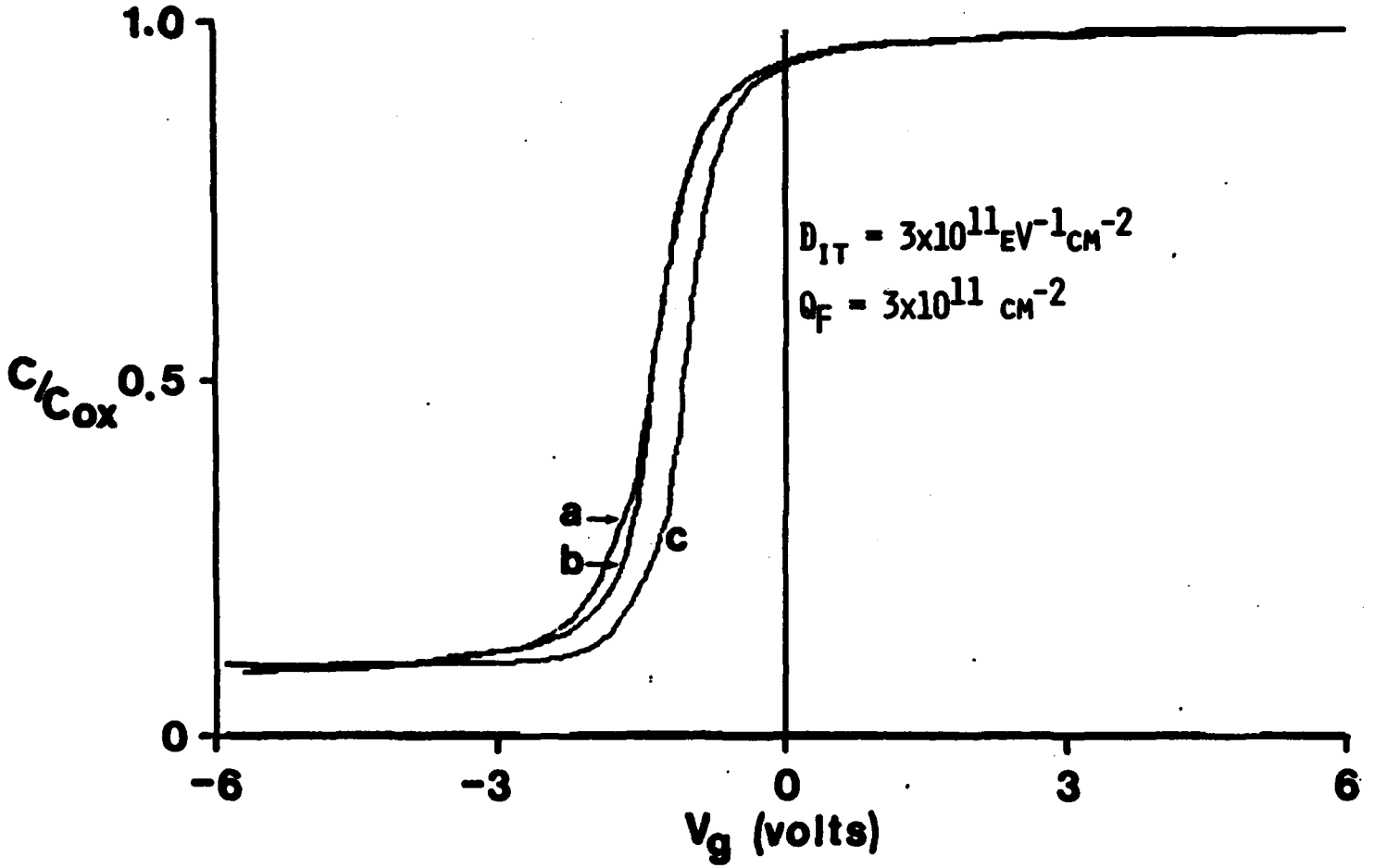
1.0
0.5
0
C/C_ox
D_IT = 3x10^11 eV^-1 cm^-2
Q_F = 3x10^11 cm^-2
a
b
c
-6
-3
0
3
6
V_g (volts)

Fig. 8, p. 29

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REPORT DOCUMENTATION PAGE

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1. REPORT NUMBER	2. GOVT ACCESSION NO. N/A; 3. RECIPIENT'S CATALOG NUMBER N/A
4. TITLE (and Subtitle): Electrical Properties of 10-50 nm TEOS LPCVD Films	5. TYPE OF REPORT & PERIOD COVERED: Technical Report - 26 October 1980 through 25 April 1984; 6. PERFORMING ORG. REPORT NUMBER
7. AUTHOR(s): R.H. Vogel, S. R. Butler, and F. J. Feigl	8. CONTRACT OR GRANT NUMBER(s): DAAG29-81-K-0007
9. PERFORMING ORGANIZATION NAME AND ADDRESS: Sherman Fairchild Center for Solid State Studies, Lehigh University, Bethlehem, PA. 18015 USA	10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS
11. CONTROLLING OFFICE NAME AND ADDRESS: U. S. Army Research Office, Post Office Box 12211, Research Triangle Park, NC 27709	12. REPORT DATE: 24 August 1984; 13. NUMBER OF PAGES: 29
14. MONITORING AGENCY NAME & ADDRESS(if different from Controlling Office)	15. SECURITY CLASS. (of this report): Unclassified; 15a. DECLASSIFICATION/DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT (of this Report)

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18. SUPPLEMENTARY NOTES

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19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Metal-Oxide-Semiconductor Devices, VLSI, Chemical vapor deposition, Tetraethoxysilane, Thin oxide films, Oxide charge, Interface states and traps

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

Silicon dioxide films deposited at 700°C from the pyrolytic decomposition of tetraethoxysilane in a low pressure nitrogen ambient exhibited very poor electrical properties. This was due to the poor quality of both the LPCVD oxide bulk (manifest as a hysteretic instability exceeding one volt in 20 nm films) and the LPCVD oxide-silicon interface (interface trap charge and fixed charge exceeding 1E+12/cm^2). These were not improved by post-deposition annealing in nitrogen at 700°C. However, the interface characteristics were improved by post-

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20. Abstract Continued

deposition annealing in oxygen. Silicon dioxide deposited at 700°C from the pyrolytic decomposition of tetraethoxysilane in a low pressure oxygen ambient exhibited reduced values of interface trap charge and fixed charge, and an order of magnitude smaller bias instability. The interface properties of these films could be further improved by standard N_2-PDA/PMA annealing sequences known to be beneficial for thermal oxides.

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